EITHNE: A FRAMEWORK FOR BENCHMARKING MICRO-CORE ACCELERATORS

WHAT ARE MICRO-CORES?

- Micro-cores have small instructions sets and tiny amounts (c.32KB) of on-chip memory, resulting in very low power consumption.
- The low power consumption and simplicity of core mean that a large number can be placed on a chip.
- The HPC community is more and more interested in micro-core architectures as they provide massive parallelism on-chip. For example the RISC-V based European Processor Initiative (EPI), and a combination of micro-cores with normal technology for "posits".
- There are lots of hard-processor examples including the Adapteva Epiphany and the PEZY-SC2 (Shoubu system B).
- There is also an increasing number of soft-core examples, such as the GRVI Phalanx.

WHICH ONE TO CHOOSE?

There are a number of factors to consider for the selection of a soft-core for use in a micro-core accelerator:

- Performance
- Power consumption
- Chip area - complex instruction sets require large decoding logic
- Scalability - maximum clock frequency can be limited by the complexity of core design
- Code density - on-chip RAM limited

Objectives:

- Provide a framework to support benchmarking of multiple hard and soft micro-core accelerators from a single codebase
- Measurement:
  - FLOPS
  - Power consumption (Watts)
  - Code size
  - Support multiple benchmarks

Sample Results:

For expediency, we highlight a small sample of results here:

- Performance and power consumption for a single core of a subset of the supported devices
- Eithne supports multi-core devices and metrics can be created for a group / cluster of cores
- The results highlight the benefits of a 'device' is flexible: most often this is a micro-core accelerator but it could be a thread running on the host

Framework overview:

The framework provides a set API functions that enable a "plug-in" architecture to support multiple benchmarks and devices

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Sample Results:

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  - Performance and power consumption for a single core of a subset of the supported devices
  - Eithne supports multi-core devices and metrics can be created for a group / cluster of cores
  - The results highlight the benefits of a framework that supports a number of different micro-cores and communication links

Currently supported devices:

- PICORV32 (soft-core)
- VectorBlox Orca (soft-core)
- RISCY (NXP NV32M1)
- Xilinx MicroBlaze (soft-core)
- ARM
- Cortex-M1 (soft-core)
- Cortex-A9
- Adapteva Epiphany
- Intel x86-64

Further work:

- Implement additional benchmarks
- Benchmark additional RISC-V soft-cores e.g. RISCY, SweRV
- Kernels implemented using OpenMP
- MPI-based communications

Available on GitLab:

https://gitlab.com/mjamieson/eithne