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**Citation for published version:**

Abaravicius, B, Cochran, S & Mitra, S 2018, 'An area-efficient hybrid high-voltage charge pump design for IoT applications'.

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# An area-efficient hybrid high-voltage charge pump design for IoT applications

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**Abstract**— A new hybrid charge pump topology is proposed to achieve high voltage DC supply in a TSMC 0.13  $\mu\text{m}$  BCD technology. The design incorporates a hybrid cross-coupled and serial-parallel topologies which permits the use of MIM capacitors through-out the design and, thus, minimizes the overall area required for the same voltage gain. The paper proposes a new zero-reversion loss cross-coupled charge pump and a new serial-parallel charge pump design to reduce the overall area required for the charge pump by up to 50 % and provides a strong basis for different gain charge pump implementations.

**Keywords**— charge pump (CP), high voltage, IoT, MIMCAP, MOMCAP, serial-parallel, heap.

## I. INTRODUCTION

Sensors based IoT nodes are a new class device that will have a wide range of environmental and medical applications [1]. These are essentially miniature wireless sensors that either harvests power or run on a small battery. However, given the need to drive a sensor front-end, they have various supply voltage requirements. While various charge-pumps and power management circuits have been developed to boost the low harvested voltage (few hundreds of millivolts) to few volts [2][3], not much has been done to address the need for a high voltage ( $>20\text{V}$ ) on a stand-alone IoT. The size restriction on an environmental or implanted sensor makes it rather challenging to fit a high-voltage power-management-unit (PMU) on such a device. Considering a 3V Li-Ion battery, we designed the core charge-pump necessary for such a PMU.

Such high voltages are necessary for flash memory[4], MEMS oscillators [5], ISFET [6] and SPAD-based sensors [7]. To facilitate high-voltages on a CMOS chip with low-voltage devices, various charge pump (CPs) designs have previously been reported [8] (Sec-II). However, the area consumption of a CP module is rarely a concern and external capacitors are often used for increased efficiency [xx]. In contrast, wireless sensor nodes are often restricted by their overall size. Hence, a novel area-efficient hybrid charge pump is proposed here. This consists of a cross-coupled and serial-parallel charge pump stages that addresses the issue of a limited gate oxide breakdown voltage, ensuring that  $V_{\text{GS}}$  of each MOS and voltage across pump capacitors do not exceed the technology specified limits. The design has been carried out in TSMC 0.13- $\mu\text{m}$  5V/HV BCD technology and compared to conventional Dickson and cross-coupled charge pump designs.

## II. CHARGE PUMP TOPOLOGIES

All charge pumps can be grouped into six different topologies: Cockcroft-Wilton (CW), Dickson, Fibonacci, cross-coupled (CC), exponential ( $2N$ ) and serial-parallel (heap) (Fig. 1). The highest gain with the lowest number of stages can be achieved by a  $2^N$  topology, however, this method can only be implemented in high-voltage (HV) technology that can tolerate full  $2^{N-1}$  voltage swings [9]; otherwise it has to rely on additional  $G_V$  gain limiting techniques [10]. The same HV issue arises with Fibonacci type CPs. It has been shown to have equal performance to Dickson CPs in integrated environments [11], although most of its implementations have been explored in discrete component setups [12]. The rest of the CP topologies are of linear nature and all but the serial-parallel configuration have a single  $V_{\text{DD}}$  drop across their switches. Although only CW and SP charge pumps have a single  $V_{\text{DD}}$  drop across their capacitors, they are highly influenced by parasitic capacitances. Hence, only a few designs being produced over the years that utilised CW [13] or SP principles [14]. Dickson and cross-coupled topologies have the highest efficiencies and are also the most popular CP design techniques.

TABLE I. DIFFERENT CHARGE PUMP TOPOLOGY PARAMETERS

	VMAX Gain (GV)	Current Efficiency	VCAP (Max)	VSW (Max)
Cockcroft-Wilton	$N + 1$	$1/GV$	1	1
Serial-Parallel			1	N
Cross-Coupled			N	1
Dickson			N	1
Fibonacci	$F(N+1)$		$F(N-1)$	
$2N$	$2N$		$2N-1$	

Fig. 1 Voltage and current gain, switch and pumping capacitor ratings of different topologies.

### A. Pumping Capacitor Area and Parasitic Effects

The issue with both Dickson and cross-coupled CPs is that they expose capacitors to a progressively higher voltage with each subsequent stage. The switching capacitance for further steps cannot be implemented using Metal-Insulator-Metal (MIM) or Metal-Oxide-Semiconductor (MOS) capacitors which are limited by the technology specification; only Metal-Oxide-Metal (MOM) capacitors

can be used. MOM capacitors consist of multiple interdigitated lines, the distance between which defines the voltage tolerance of the device. MOM capacitor total capacitance depends on the number of metal layers used and the capacitive/area can come close to that of a MIMcap if all of the available layers are utilised. The downside of this approach is a much higher parasitic capacitance due to the proximity to the substrate.

In TSMC 0.13  $\mu\text{m}$  technology, a 1.5 fF/ $\mu\text{m}^2$  MIMcap is available which is implemented in the fifth and sixth metal layers of the chip. A 1.4 fF/ $\mu\text{m}^2$  MOMcap is also available if all (1-5) metal layers are used. Although the two capacitances are similar, the MOMcap implementation requires the full stack of the five available metal layers. In contrast, the use of MIMcaps permits the full charge-pump circuitry to be implemented under the switching capacitors. For a four stage CP with an input voltage being the maximum tolerable technology limit), this results in a maximum of 43% area reduction in comparison to a MOMcap implementation. It is important to note that if fewer layers are chosen for the MOMcap to reduce parasitic effects or other reasons, the area saved increases even further.

### B. Serial-parallel Charge Pump

The TSMC BCD technology permits the use of high voltage devices of up to 36 V and, thus, a serial-parallel (SP) CP is possible solution to explore. As discussed earlier, the charge pump has only a single  $V_{\text{DD}}$  drop across pump capacitances: MIM capacitors can be used.

A basic SP pump diagram can be seen in the Fig. 2. The charge pump consists of  $N$  stages each comprising of a capacitor ( $C_i$ ) and two switches ( $S_A$  and  $S_B$ ). In a conventional topology all capacitors are of the same size, although attempts have been made to improve the efficiency by scaling the capacitors differently [15].

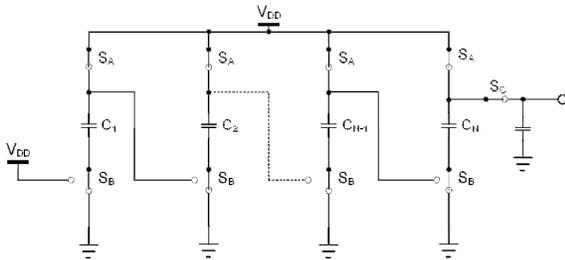


Fig. 2 A basic serial-parallel charge pump structure.

The charge pump operates in a two-phase manner. In the first phase, all capacitors are connected in parallel and are charged to  $V_{\text{DD}}$ : all  $S_A$  are turned on, all  $S_B$  are connected to ground and all  $S_C$  is off. To transition to the second phase, switches  $S_A$  are turned off,  $S_B$  are connected to top plates of preceding stage capacitors and  $S_C$  is connected to the output. After the transition each of the capacitors are connected in series, each with a  $V_{\text{DD}}$  drop across its plates; each  $S_A$  has a voltage drop of  $(k - 1) * V_{\text{DD}}$  and each  $S_B$  switch – a drop of  $k * V_{\text{DD}}$ , where  $k$  is the stage number. As a result, high-voltage switches are required.

The greatest disadvantage of the SP charge pump is a greater contribution of parasitic capacitances. This is because only a single input to provide current for all stages in series phase. It has been shown that these losses are proportional to  $N^2$  and, thus, a maximum number of stages exists for which output current drops to zero.

### III. HYBRID CHARGE PUMP

In this technology, the proposed hybrid charge pump seen in Fig. 3 can overcome the problems of a dedicated SP, CC or DW architecture and provide the most optimum area usage. The design consists of two cascaded subcircuits: a cross-coupled (CC) charge pump (CP) and a serial-parallel (SP) CP and was designed to be powered from two 1.55 V silver oxide batteries (3.1 V total). It utilises a regulated high-efficiency cross-coupled voltage doubler to multiply the input voltage up to  $V_{\text{OUTCC}}$  which is limited by the oxide breakdown limit, specified to be 5.5 V of the low-voltage transistors. This voltage is then supplied to a four stage SP CP (using high-voltage transistors) to achieve output voltage of more than 20 V, under a 20  $\mu\text{A}$  load.

The hybrid implementation runs the two sub-CPs at different operational frequencies. It has been observed that the SP CP operates more efficiently with a high value pumping capacitance and lower frequency, however, in such a condition a high pumping capacitance for the CC stage is also necessary. To minimise the total CP area, CC CP runs at a much higher frequency (15 – 30 MHz), whilst the SP CP is operating 15 - 30 times slower. The regulation at the output of the CC CP, besides limiting its output voltage, has two additional benefits. Firstly, it ensures that the CC CP adjusts to different SP CP current draw requirements for different output voltages. Secondly, the SP CP has different current requirements in parallel and series phases, drawing at least  $(N-1)$  times more current in parallel stage, where  $N$  is the number of stages. Regulation ensures that the duty cycle of the CC CP is adjusted for different SP CP phases and so it optimizes power consumption for any given load. A feedback can be included to regulate output of the SP CP as well, although for the highest efficiency it is better to design the SP CP for a specific load current and operate it continuously.

#### A. Zero-Reversion Loss Cross-Coupled Stage

The cross-coupled stage has been chosen for the first part of the circuit due to its highest efficiency amongst other CP topologies. A no-reversion loss design has been implemented that utilises an auxiliary circuit (Fig. 3, red box) similar to the one used in [16]. The auxiliary circuit is a smaller cross-coupled voltage doubler with its outputs connected to the main CP nMOS ( $M_{\text{CC1}}$  and  $M_{\text{CC2}}$ ). The size of the auxiliary circuit pumping capacitors  $C_{\text{CC1}}$  and  $C_{\text{CC2}}$  depends on the gate capacitance of  $M_{\text{CC1/CC2}}$ : the smallest it can be determined by the minimum gate voltage  $V_G = V_{\text{DD}} + V_{\text{THN}}$  that has to be applied to turn the nMOS on. In the timing diagram it is shown as  $2V_{\text{DD}}$  for simplicity. At the same time,  $C_A$  and  $C_B$  are much larger and can easily boost  $V_G$  of  $M_{\text{CC2/CC1}}$  up to  $2 V_{\text{DD}}$ . The cross-coupled implementation does not have any other inverters and has no

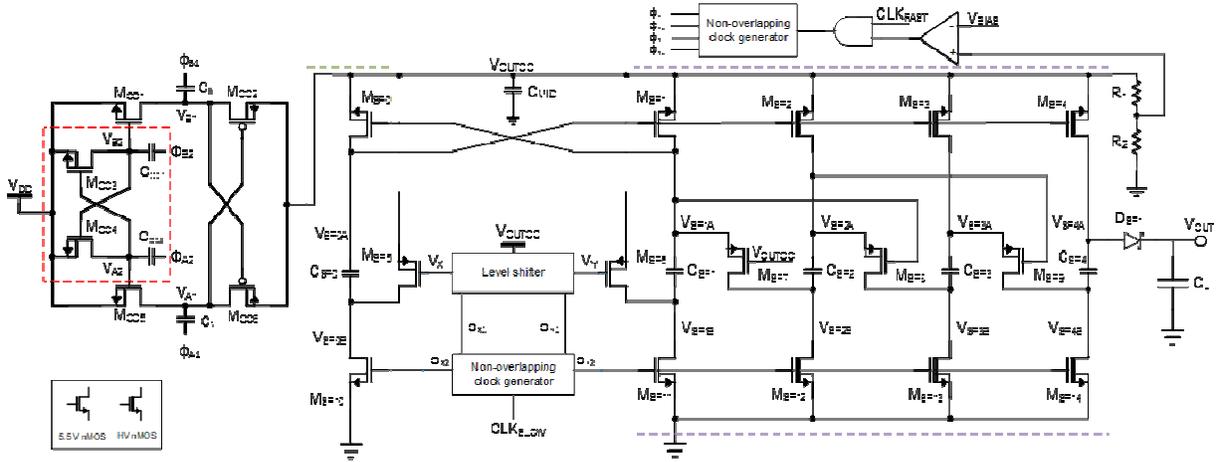


Fig. 3 Schematic of the proposed hybrid CP.

reversion losses in the auxiliary circuit either. The cross-coupled CP utilizes 5 V devices in a deep n-well, biased at a  $V_{DD}$ .

The timing diagram of the charge pump can be seen in Fig. 4 (left). The operation under stable conditions can be described as follows:  $\phi_{A2}$  goes low and  $M_{CC5}$  is turned off,  $\phi_{A1}$  goes high and  $V_{A1}$  is boosted to  $2V_{DD}$ ; at the same time  $V_{A1}$  disables  $M_{CC2}$ . The charge remains at the node as both  $M_{CC5}$  and  $M_{CC6}$  are turned off. Consequently, clock  $\phi_{B1}$  drops low,  $V_{B1}$  drops to  $V_{DD}$  and the  $V_{A1}$  node is connected to the output. Finally, clock  $\phi_{B2}$  goes high, enabling  $M_{CC1}$  and charging  $V_{B1}$  to  $V_{DD}$ . The cycle ensures that at any time the flying capacitors are connected to only the input or the output nodes; this is done only before the node is brought to the appropriate voltage level:  $V_{DD}$  before input and  $2V_{DD}$  for the output.

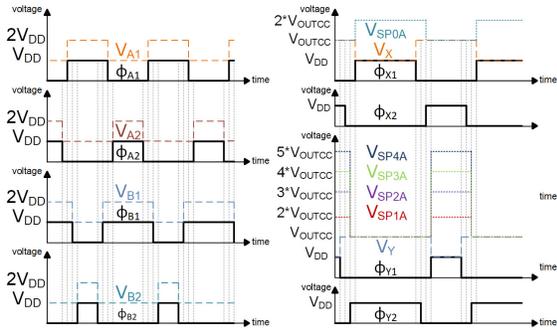


Fig. 4 Timing diagram of cross-coupled (left) and serial-parallel (right) charge pumps.

### B. Serial-parallel Charge Stage

The proposed SP CP consists of the main SP pump (Fig. 3, purple box) and two auxiliary circuits: a cross-coupled CP with an inverter (blue box) and an extra CP branch cross-coupled with the first stage of the SP pump (green box). The auxiliary cross-coupled CP boosts the clock ( $\phi_{X1}$  and  $\phi_{Y1}$ ) and controls the gate voltage of  $M_{SP6}$  and  $M_{SP7}$  that varies

between  $V_{DD}$  and  $V_{OUTCC}$ . At the same time, the extra pump branch ( $C_{SP1}$ ,  $M_{SP1/SP11}$ ) coupled to the first stage of the main pump is used to control the nMOS in the main pump -  $M_{SP2-SP5}$ . As both auxiliary circuits control only the gate of other MOS devices, much smaller pumping capacitances can be used than in the main pump and little power loss is added.

A four phase non-overlapping clock is used to control the SP charge pump (Fig. 4 (right)). When clock  $\phi_{X1}$  goes high, node  $V_X$  will go to  $2 \cdot V_{OUTCC}$ :  $M_{SP2-5}$  are turned on and capacitors  $C_{SP1-4}$  charge to  $V_{OUTCC}$ . After charging,  $\phi_{X1}$  goes low,  $V_X$  goes high and disables  $M_{SP6}$ . Consecutively,  $\phi_{Y2}$  goes low, turning  $M_{SP12-15}$  off and isolating bottom plates of  $C_{SP1-4}$ . Clock  $\phi_{X2}$  then goes high, which connects  $V_{SP0B}$  to ground and brings  $V_{SP0A}$  to  $V_{OUTCC}$  voltage, disabling  $M_{SP2-5}$  in the process. Finally,  $\phi_{Y1}$  goes high,  $V_Y$  drops enabling  $M_{SP7}$  and connecting  $V_{SP1B}$  to  $V_{OUTCC}$ . This causes  $V_{SP1A}$  to start raising from  $V_{OUTCC}$  to  $2V_{OUTCC}$ : when  $V_{SP1A}$  increases to  $(V_{OUTCC} + V_{THP})$ , transistor  $M_{SP8}$  starts to conduct and  $V_{SP2A}$  starts raising to  $3V_{OUTCC}$ .  $V_{SP1A}$  and  $V_{SP2A}$  continue to raise simultaneously which ensures  $V_{GS}$  of  $M_{SP9}$  to remain lower than  $V_{OUTCC}$ . The same mechanism causes voltage to raise throughout the whole CP, however, due to threshold of each pMOS, a small delay is added with each stage. The difference is not significant between the first and second stages, but could cause an overvoltage condition between stages two and three.

## IV. RESULTS

To compare circuits with higher confidence, MIMcap and MOMcap parasitic effects were included in schematic simulations. MIMcap parasitic effects could be ignored for the top layer and the bottom plate effects were acquired by extracting parasitic coupling between layers M4/5 of a  $40 \mu\text{m} \times 40 \mu\text{m}$  metal plates (equivalent to  $2.42 \text{ pF}$  MIMcap) resulting in a  $1.3 \%$  parasitic coupling. This number was rounded up to  $1.5 \%$  to include additional losses lines switching devices. MOM capacitors available in TSMC  $0.13\text{-}\mu\text{m}$  were equivalent to the  $30 \text{ V}$  tolerance devices used in [17] with total of  $8.8 \%$  parasitic capacitance.

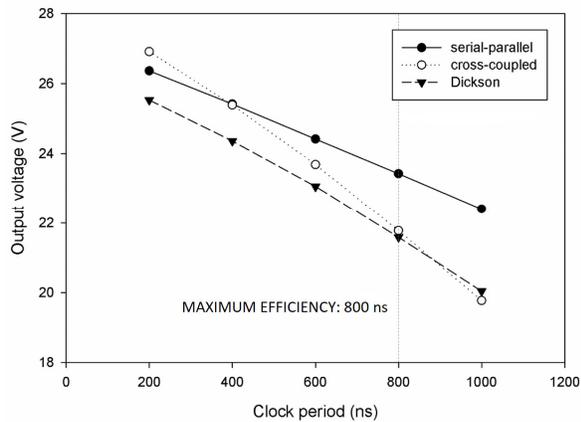


Fig. 6 Output voltage of the proposed hybrid charge pump

Fig. 6 shows comparison of the output voltage versus operating clock period of four stag CPs. Three topologies occupying the same area (with parasitic effects included) and with an output current of  $20 \mu\text{A}$  are compared. A  $15\text{pF}$  MIMcap pumping capacitance was chosen for the SP CP and the capacitor area were scaled down for Dickson (20%) and CC (30%) charge pumps to accommodate larger MOM caps. SP reaches a peak efficiency of 54 % whilst Dickson and CC achieve 55 %, however, output voltage is much higher for the SP implementation. It can be concluded that for the same area the design achieves a better performance and, thus, the area can be reduced to achieve similar efficiency with a decrease in the overall pump area. The Fig. 5 depicts the output transient response of the overall hybrid CP design for different output currents.

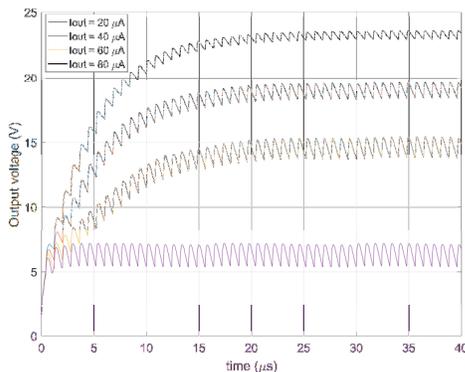


Fig. 5 Output voltage of the hybrid CP for different output

## V. CONCLUSIONS AND ACKNOWLEDGEMNT

The newly proposed hybrid CP is comprised of two subcircuits: a high efficiency cross-coupled and SP charge pumps that utilise low-voltage metal-insulator-metal capacitors. The design addresses the main issue of a high voltage CP implementation in TSMC BCD technology within the oxide-breakdown limit and improves the overall CP area consumption. Based on schematic simulations and including parasitic effects of different integrated capacitors, it was concluded the design is a competitive alternative to

fully Dickson or cross-coupled based designs for HV applications.

This work was supported by PhD fellowship from Dialog Semiconductor, Edinburgh. The authors are grateful for constructive feedback from Jim Brown and Guillaume Decremoux.

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